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09/680,334	10/06/2000	Peter Brian Wilson	550-183	9108
23117	7590	10/05/2004	EXAMINER	
NIXON & VANDERHYE, PC 1100 N GLEBE ROAD 8TH FLOOR ARLINGTON, VA 22201-4714			DESTA, ELIAS	
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Examiner's Answer

**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 09/680,334  
Filing Date: October 6, 2000  
Appellant(s): Wilson

**MAILED**  
OCT 05 2004  
**GROUP 2800**

John R. Lastova  
For Appellant

### **EXAMINER'S ANSWER**

1. This is in response to the appeal brief filed May 21, 2004.

### **Real Party in Interest**

2. A statement identifying the real party in interest is contained in the brief.

### **Related Appeals and Interferences**

3. A statement identifying the related appeals and interferences, which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

### **Status of Claims**

4. The statement of the status of the claims contained in the brief is correct.

### **Status of Amendments After Final**

5. The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

### **Summary of Invention**

6. The summary of invention contained in the brief is correct.

### **Issues**

7. The appellant's statement of the issues in the brief is correct.

### **Grouping of Claims**

8. Appellant's grouping of claims statement is correct.

### **Claims Appealed**

9. The copy of the appealed claims contained in the Appendix to the brief is correct.

### **Prior Art of Record**

10. The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,731,839 PANARO 03-1998

### **Grounds of Rejection**

11. The following ground(s) of rejection are applicable to the appealed claims:

#### **Claim rejection – 35 U.S.C. 102**

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1, 4 and 11-13 are rejected under 35 U.S.C. 102(b) as anticipated by Panaro (U.S. Patent 5,731,839).

In reference to claim 1: Panaro teaches a method of generating test bit stream to test a bit-stream decoder arranged to decode bit-streams generated in accordance with a predefined syntax (a MPEG coding algorithm is used to generate the test bit stream) (see Panaro, column 2, lines 32-37), including the steps of:

- Generating test code from the syntax (see Panaro, column 1, lines 24-31) where a discrete cosine transform algorithm is used to form typical bit streams, the test code (which is the encoded particular test image) being arranged when executed to generate a test bit-stream dependent on values assigned to a plurality of variables (or set of vectors) (see Panaro, column 6, lines 34-45), each variable having a number of interesting values (magnitude and direction) (see Panaro, column 2, lines 20-45);
- As noted above, executing the test code (the discrete cosine transform, see column 6, lines 34-45) including the step of, for each variable, assigning that variable one of its interesting values

(predefined pixel values), thereby generating a test bit-stream dependent on the interesting value (magnitude and direction) assigned to each variable or vector (see Panaro, column 3, line 50 to column 4, line 37); and

- Panaro further teaches that executing the test code is repeated until each variable has been assigned because to create the B frame both the first and second P-frames are utilized and then each of the B frame or interesting (predetermined) values are used to generate sets of bit-stream values (see Panaro, Fig. 3 and column 5, lines 33-55).

With regard to claim 4: as noted above in claim 1, Panaro further teaches that the variable is defined by the syntax (see Panaro, column 1, lines 27-38).

In reference to claim 11: Panaro teaches a test bit-stream generator for generating test bit-streams to test a bit-stream decoder arranged to decode bit-streams generated accordance with a predefined syntax where the MPEG algorithm is used to generate the test bit-stream (see Panaro, see Panaro, column 2, lines 32-37). The system includes:

- A processor arranged to execute test code generated from the syntax (see Panaro, column 1, lines 24-31) where a discrete cosine transform algorithm is used to form typical bit streams, the test code (which is the encoded for particular test image) being

arranged when executed to generate a test bit-stream dependent on values assigned to a plurality of variables (or set of vectors) (see Panaro, column 6, lines 34-45), each variable having a number of interesting values (magnitude and direction) (see Panaro, column 2, lines 20-45);

- A value determination means, responsive to execution of the test code (see Panaro, column 4, lines 1-37), to assign to each variable one of the interesting values, where a test bit-stream is generated dependent on the interesting value assigned to each variable (the B and P frames).

With regard to claim 12: as noted above in claim 1, Panaro further teaches that the system includes a computer program operable to configure a processing unit to perform a method of generating test bit-streams because Panaro in column 3, lines 41-49 indicates that the decoder under test can be implemented as a software decoder (see also Panaro, Fig. 1). Fig. 1 includes a computer (100) with input devices (106), a decoder under test (108), and a video display (110). Hence, a computer program is necessarily present to generate the test bit stream using discrete cosine transforms (see Panaro, column 6, lines 34-46)

With regard to claim 13: as noted above in claim 12, Panaro further teaches that the carrier medium includes interface hardware between

display/input devices and the main computer (see Panaro, Fig. 1, member 104, 106 and 108).

### **Allowable Subject Matter**

14. Applicant's arguments, in the brief filed May 21, 2004, regarding claims 3 and 5-10 have been fully considered and are persuasive. The rejection of the claims noted above has been withdrawn. However, Claims 3 and 5-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### **Response to Argument**

15. The Examiner disagrees with the assertion that Appellant's claims are distinguishable from Panaro.

In reference to claim 1: Appellant indicates that the instant case provides a means to generate test code from a "predefined syntax". A "predefined syntax" is one of the characteristics of MPEG encoding scheme (see CRC, section 18.1 and 8.3.2). Therefore, as discussed in Panaro, column 2, lines 20-37, especially lines 35-37 indicate that the predictive encoder particularly an MPEG coding algorithm is used to form the test bit stream. Panaro further includes a set of motion vectors having predefined characteristics, hence these vectors having

magnitude and direction provide a plurality of variables that define the interesting values or the test bit streams (see Panaro, column 2, lines 20-37).

Further, Panaro teaches the steps to assign each interesting values, because to create the B frame both the first and second P-frames are used and then each of the B frame or interesting (predetermined) values are used to generate sets of bit-stream values (see Panaro, Fig. 3 and column 5, lines 33-55).

Panaro teaches (1) each variable (the motion vectors) having multiple interesting values, and (2) repeating execution of the test code until the test code has been exhausted multiple times with each variables having been assigned each of its interesting values because in column 5, lines 33-55 Panaro teaches that the method uses an error detection method which includes a repeated B-frames for a number of times. For instance, the example given in Panaro where the test frames in the completed decoded image sequence start with I-frames followed by P-frame, fifteen B-frames and another P-frame where the entire sequence is used to form the test bit stream. Hence, the sequence represents multiple values and has a repeated sequence.

With regard to claim 11, as noted above and shown in Fig. 2 of Panaro, the bit stream generation routine (member 200) provides a means to generate bit streams. The means generates the bit streams based on the predefined syntax because the system uses MPEG encoding scheme. The system includes a

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processor (Fig. 1, CPU) arranged to execute test code (see the discussion in claim 1 and 11 above) where the codes reside in the RAM (member 116), value determination means that is shown again with the CPU where the output is provided to the viewer through video display 110.

With regard to claims 12 and 13: as noted above in claim 11, Panaro further teaches that the system also includes a computer program operable to configure a processing unit to perform a method of generating test bit-streams because Panaro in column 3, lines 41-49 indicates that the decoder under test can be implemented as a software decoder (see also Panaro, Fig. 1).

### Conclusion

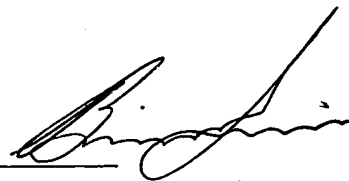
16. For the above reasons, it is believed that the rejections to the applicable claims should be sustained.

Respectfully submitted,

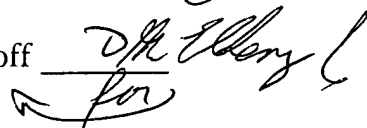
E.D, August 12, 2004

#### Conferees

- Brian Sircus



- Marc S. Hoff



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